Evaluation Board for Low Cost, Low Power, CMOS Gerneral Purpose Analog Front End

EVAL-AD73311EB

FEATURES

Up to 4 CODECS Can Be Configured In Cascade.

Interfaces To The ADSP-2181 EZ-KIT LITE.

Stand Alone Capabiliy.

Daughter Board for Quick Demo of CODECS

Various Link Options For Setting Configuration.

On Board +5V Regulator.

On Board Clock Generator.

On Board Anti-Aliasing.

MODIFYING AN EXISTING EZ-KIT LITE BOARD:

An exixting EZ-KIT LITE board can easily be modified to interface with the EVAL-AD73311EB board by carrying out the following modification:

1. Solder the 40 pin right angle header (included in the EVAL-AD73311EB package) onto the EZ-KIT LITE board in position P3, pins 11-50, with the header pins facing the edge of the board.

INTRODUCTION

The AD73311 is a complete front-end processor for general purpose applications including speech and telephony. It features a 16-bit A/D conversion channel and a 16-bit D/A conversion channel. Each channel provides 70 dB signal-to-noise ratio over a voiceband signal bandwidth. The final channel bandwidth can be reduced, and signal-to-noise ratio improved, by external digital filtering in a DSP engine.

The AD73311 is suitable for a variety of applications in the speech and telephony area including low bit rate, high quality compression, speech enhancement, recognition and synthesis. The low group delay characteristic of the part makes it suitable for single or multichannel active control applications.

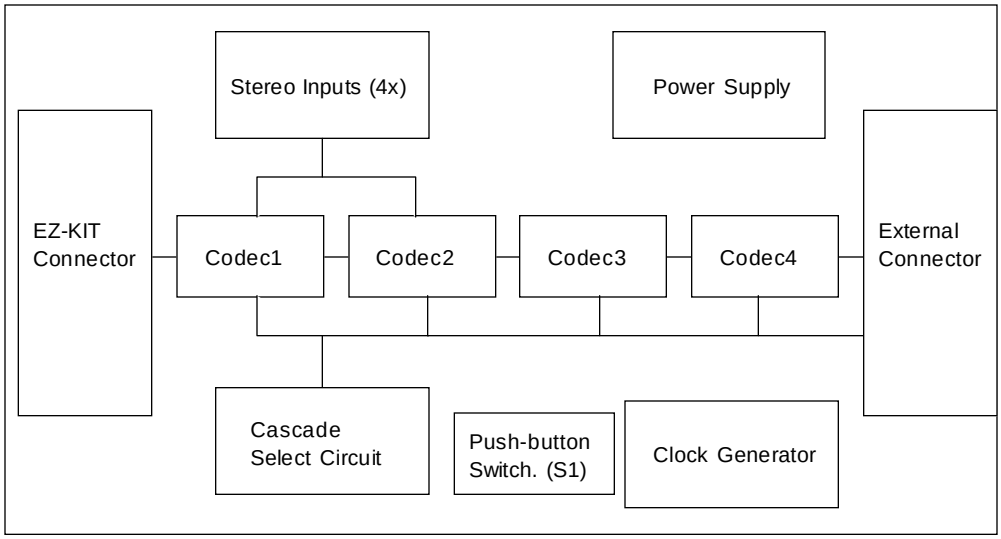
The gains of the A/D and D/A conversion channels are programmable over 38dB and 21dB ranges respectively. An on-chip reference voltage is included to allow single supply operation. A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines.

The AD73311 is available in both 20-pin SOIC and SSOP packages.

Full data on the AD73311 is available in the AD73311 data sheet available from Analog Devices and should be consulted in conjunction with this Technical Note when using the Evaluation Board.

Included on the evaluation board, along with the four AD73311 Codecs are a power supply circuit, a clock generator circuit, a cascade selector circuit and a daughter board. These are explained in detail on the next page.

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood. MA 02062-9106, U.S.A.
Tel: 617/329-4700 *Fax: 617/326-8703*

Power Supply Circuit.

D.C. power between 8V & 12V is applied to the board through either connector P1 or P3 (positive is on the outer sleeve). These connectors are connected together in a loop through arrangement which is intended for supplying the external voltage to the EZ-KIT LITE which accompanies this evaluation board. The power supply shipped with the EZ-KIT Lite is suitable for powering both the AD73311 board and the EZ-KIT LITE board. Diode, D1, prevents damage due to accidental reversal of the supply. Regulator, REG1, generates the +5V necessary for all the analog and digital circuitry on the board.

Clock Generator Circuit.

The oscillator, X1, provides two stable crystal controlled outputs of 16.384MHz or 8.192MHz. One of these frequencies is selected by JP13 to produce the on-board generated clock signal. JP12 is used to select this clock signal or the EZ-KIT LITE clock signal as the master clock (MCLK). MCLK is used as the main clock for the AD73311 and is also used for the external synchronisation circuit for the SE and $\overline{\text{RESET}}$ signals. The board is shipped with 16.384MHz selected as the default clock frequency.

Cascade Selector circuit.

This is programmed by software to determine the number of codecs in cascade. The 74HC253(U8) is a 2 channel 4-1 multiplexer which is automatically controlled by software to select which codec has its SDO and SDOFS returned to the DSP. The process of downloading a user program automatically sets the multiplexer to the required setting.

Daughter Board.

The main function of the daughter board is to provide immediate functionality of the DEMO SYSTEM by providing a stereo line or microphone input and buffered output. Op-amps U1A & U2A provide a high impedance input for an external microphone. Op-amp U1B buffers the reference from the codecs to provide phantom power to a microphone if necessary. Op-amp U3 forms a dual differential to single ended converter which takes the high impedance differential output from the codecs to a low impedance for driving headphones or powered speakers. The circuit diagram and component placement drawing for the Daughter Board are shown in figures 4 and 7. The daughter board mates with the main board via headers JP1, JP2, JP5 & JP6.

Jumpers LK1 and LK2 in the A position direct the inputs to the buffers. Jumpers LK1 & LK2 in the B position allow a direct line in to the codecs. Jumpers LK3 & LK4 allow phantom power to be provided to a non powered microphone.

OPERATING THE AD73311 EVALUATION BOARD

The AD73311 EVAL BOARD is designed to be interfaced directly to the EZ-KIT LITE which is an entry level demonstration tool for the ADSP-2181 DSP. The interface to the EZ-KIT LITE is provided through the connector J5. Alternatively, the board may be connected to the Texas Instrument TMS320C5XX EVM via connector J7.

Before applying power and signals to the evaluation board it is essential to ensure that all links are set as required for the desired operating mode. The function of all links is explained below.

Link	Board	Function
JP9	Main Board	Connects TFS to RFS on DSP.
JP10	Main Board	Connects SE to VDD or FL0 of DSP.
JP11	Main Board	Connects $\overline{\text{RESET}}$ to FL2 or $\overline{\text{FL2}}$ of DSP.
JP12	Main Board	Selects the on-board generated clock or DSP clock as the master clock for the board.
JP13	Main Board	Selects between the 16.384MHz or 8.192MHz outputs from the on-board clock circuit.
JP14	Main Board	Connects the DSP signal ground to the GND plane on the Eval Board.
LK1,LK5	Daughter Board	Used to select buffered or line input to CODEC 1 .
LK2,LK6	Daughter Board	Used to select buffered or line input to CODEC 2 .
LK3	Daughter Board	Used to supply phantom power to MIC 1.
LK4	Daughter Board	Used to supply phantom power to MIC 2.

Boards are shipped with the following link settings.

LINK NO.	POSITION	FUNCTION
JP9	1 to 2	TFS tied to RFS.
JP10	1 to 2	SE tied to FL0 of DSP.
JP11	1 to 2	RESET tied to FL2 of DSP.
JP12	1 to 2	CLK tied to on board oscillator.
JP13	1 to 2	16.384MHz selected as the output of the crystal oscillator.
JP14	Inserted	DSP Signal GND connected to Eval Board GND.
LK1,LK5	A	INPUT 1 buffered.
LK2,LK6	A	INPUT 2 buffered.
LK3	IN	Phantom power to MIC 1.
LK4	IN	Phantom power to MIC 2.

INTERFACING TO THE EZ-KIT LITE

The EZ-KIT LITE shipped with this evaluation board has been modified by the inclusion of a right-angled male header strip (20 x 2) in positions 11 to 50 of connector P3. This header mates to a matching female connector (J5) on the AD73311 Evaluation board.

- Connect the AD73311 EVAL BOARD to the EZ-KIT LITE BOARD using J5.
- Plug the daughter board onto the EVAL BOARD using JP1, JP2, JP5 and JP6.
- Connect the serial cable between PC and EZ-KIT LITE.
- Attach the power loop through cable between P3 of the EVAL BOARD and the power input of the EZ-KIT BOARD.
- Apply power to the setup via P1 using the DC PSU supplied with the eval board.

When power is applied the green LED on EZ-KIT BOARD should remain lit while red LED should flash to indicate system is ready to accept a program. If any difficulty is experienced please refer to the EZ-KIT LITE REFERENCE MANUAL.

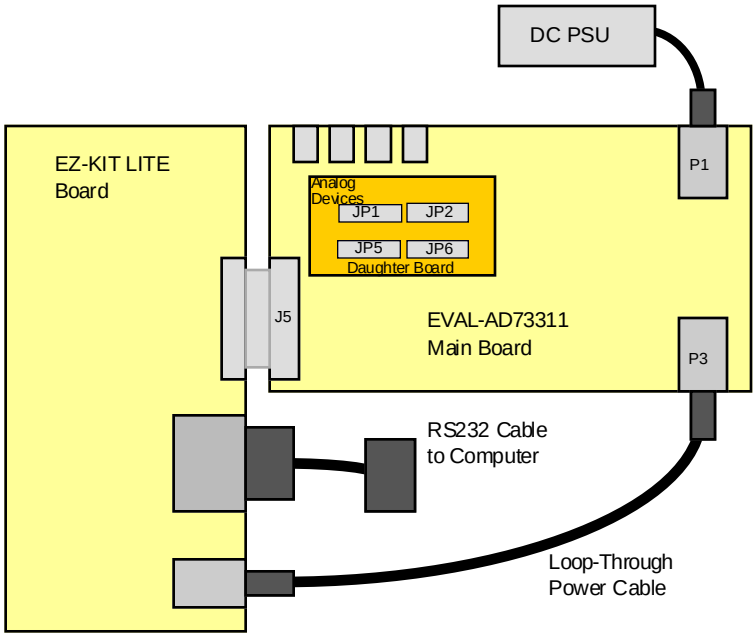


Fig. 1: Interfacing to the EZ-KIT LITE.

Analog I/O.

The analog I/O to each codec is designed to be flexible and the evaluation board provides some prototyping space for user supplied input/output circuitry. Codecs 1 and 2 use a pair of stereo (3 pole) 3.5 mm miniature jack plugs (J1 through J4) to connect signals to/from the evaluation board via single-in-line sockets JP1 and JP2 and from the prototyping space through JP5 and JP6. Codecs 3 and 4 use single-in-line sockets JP3 and JP4 and from the prototyping area through JP7 and JP8.

LOADING DEMO PROGRAMS.
Follow EZ-KIT instructions for installation of EZ-KIT software. Activate the windows FILE MANAGER and create a directory for the AD73311 diskette (example C:\ADI_DSP\EZ-73311) Copy the contents of the AD73311 demo programs diskette into this directory. Alternatively the demo programs can be run from the diskette drive. Close down FILE MANAGER.

The AD73311 evaluation board uses the user program facility of the EZ-KIT LITE PC based software to download its demonstration programs. Therefore it does not have a menu of demonstration options but instead the various demonstrations must be downloaded as one would download a user program under the existing EZ-KIT LITE software. Please refer to the EZ-KIT LITE reference manual for more details of this feature (page 6-13).

Activate the EZ-KIT LITE -Monitor host program and select the LOADING option. The red LED on the EZ-KIT LITE board must be flashing while doing this operation. Use the RESET button on the EZ-KIT board to make the LED flash if necessary.

From this select the DOWNLOAD USER PROGRAM AND GO menu. This opens the window shown in Fig. 2.

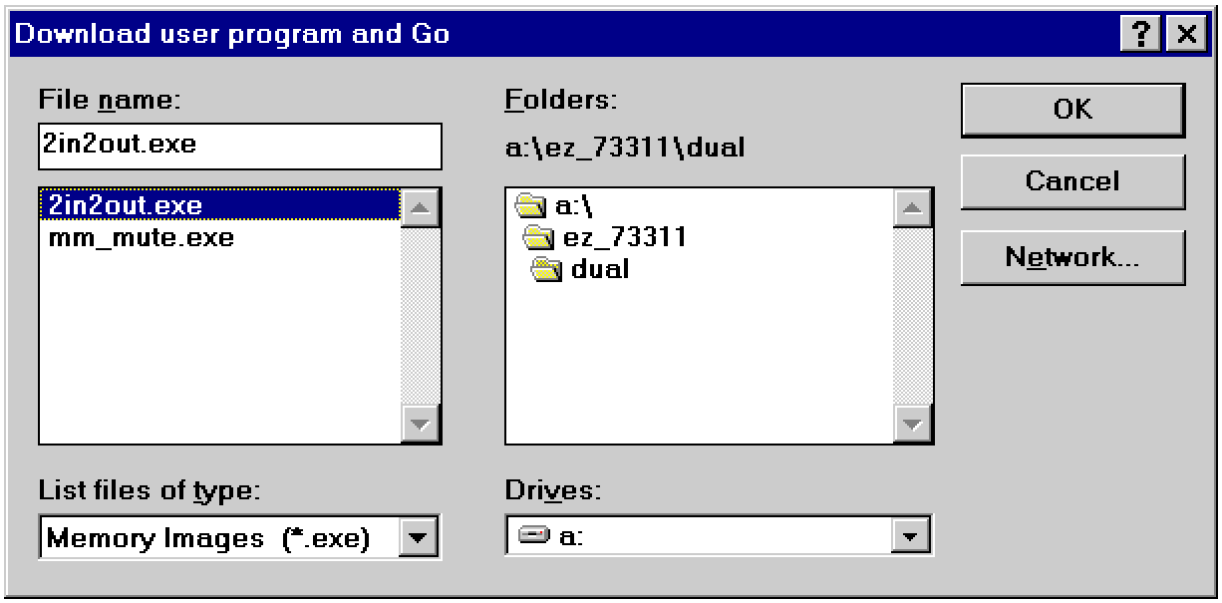


Fig. 2: Download User Program and Go menu

AD73311 SINGLE CODEC DEMO PROGRAMS

Loop-Through (64 kHz) (a:\EZ_73311\single\1in1out.exe)
In this demo a single AD73311 codec is configured for loop-through operation with input samples being passed through to the output at a 64 kHz rate. This sampling rate gives low group delay sampling which is suitable for active control applications.

Loop-Through (8 kHz) (a:\EZ_73311\single\up_dwn.exe)
This demo is similar to the 64 kHz sampling demo except that the 64 kHz sampling rate is decimated to 8 kHz rate for input which is subsequently interpolated back to 64 kHz for output. The decimation and interpolation filters provide a 4 kHz lowpass filter function as well as decimation and interpolation which increases the Signal/Noise ratio in the 4 kHz band.

Tone Generator (a:\EZ_73311\single\up_samp.exe)
This demo generates a 1 kHz tone by updating a function generation algorithm at an 8 kHz rate. The resulting output samples are interpolated from 8 kHz to the codec's output sampling rate of 64 kHz.

DTMF (a:\EZ_73311\single\dtmf\dtmf.exe)
This program uses the DAC section of the CODEC to output a series of Dual-Tone Multi-Frequency (DTMF) tones which are used in telephony applications. There are two possible settings for this demo

1 Generate a dial tone (the default setting) indicated by the LED on the EZKIT board being OFF

2 Generate a series of tones corresponding to a telephone number to be dialled indicated by the LED on the EZKIT board being ON.

Use the pushbutton (S1) on the AD73311 eval board to toggle between the two options. To close the demo please push the INTERRUPT button on the EZKIT board to return to the monitor program. This program processes output samples at an 8 kHz rate. These samples are then interpolated to a 64 kHz rate for output to the DAC.

ADPCM (a:\EZ_73311\single\adpcm\adpcm.exe)
This program demonstrates an Adaptive Differential Pulse Code Modulation (ADPCM) algorithm providing compression to 32 kbits/sec. The AD73311 samples at 64 kHz with decimation/interpolation to/from the 8 kHz rate at which the ADPCM algorithm runs. The program allows the input/output channel to be configured for loop-through at 8 kHz or for the ADPCM algorithm to be run in a loop-through mode. The ADPCM algorithm takes the 16 bit ADC output and compresses it to an 8 bit PCM value using μ-Law coding. The 8-bit PCM value is input to the ADPCM encoder which generates a 4-bit output update value. In the loop-through, this 4-bit value is input to the ADPCM decoder whose 8-bit output is further expanded from μ-Law to 16-bit linear coding.

There are two possible settings for this demo:

1 Loop-through of input to output at 8 kHz with no compression indicated by the LED on the EZKIT board being OFF

2 Loop-through of input to output at 8 kHz featuring ADPCM indicated by the LED of the EZKIT board being ON

Use the pushbutton (S1) on the AD73311 eval board to toggle between the two options. To close the demo please push the INTERRUPT button on the EZKIT board to return to the monitor program. This program processes input and output samples at an 8 kHz rate. These samples are then decimated/interpolated from/to a 64 kHz rate.

AD73311 DUAL CODEC DEMO PROGRAMS

Stereo Emulation (a:\EZ_73311\dual\2in2out.exe)
This program configures a dual codec cascade to emulate a stereo codec in that one codec converts the right channel while the other codec converts the left channel. This program's code serves as a useful introduction to configuring the AD73311 for cascaded operation.

Mixed Mode Stereo Emulation (a:\EZ_73311\dual\mm_mute.exe)
This program configures a dual codec cascade, in mixed mode, to emulate a stereo codec in that one codec converts the right channel while the other codec converts the left channel. The mixed mode mode function allows the codecs to be controlled while processing ADC and DAC samples. In this demo the pushbutton switch (S1) toggles the outputs between MUTE OFF and MUTE ON. The red LED on the EZKIT LITE board is ON when MUTE is enabled.

AD73311 MULTI CODEC DEMO PROGRAMS

Three Channels (a:\EZ_73311\multi\3in3out.exe)
This program configures a three codec cascade.

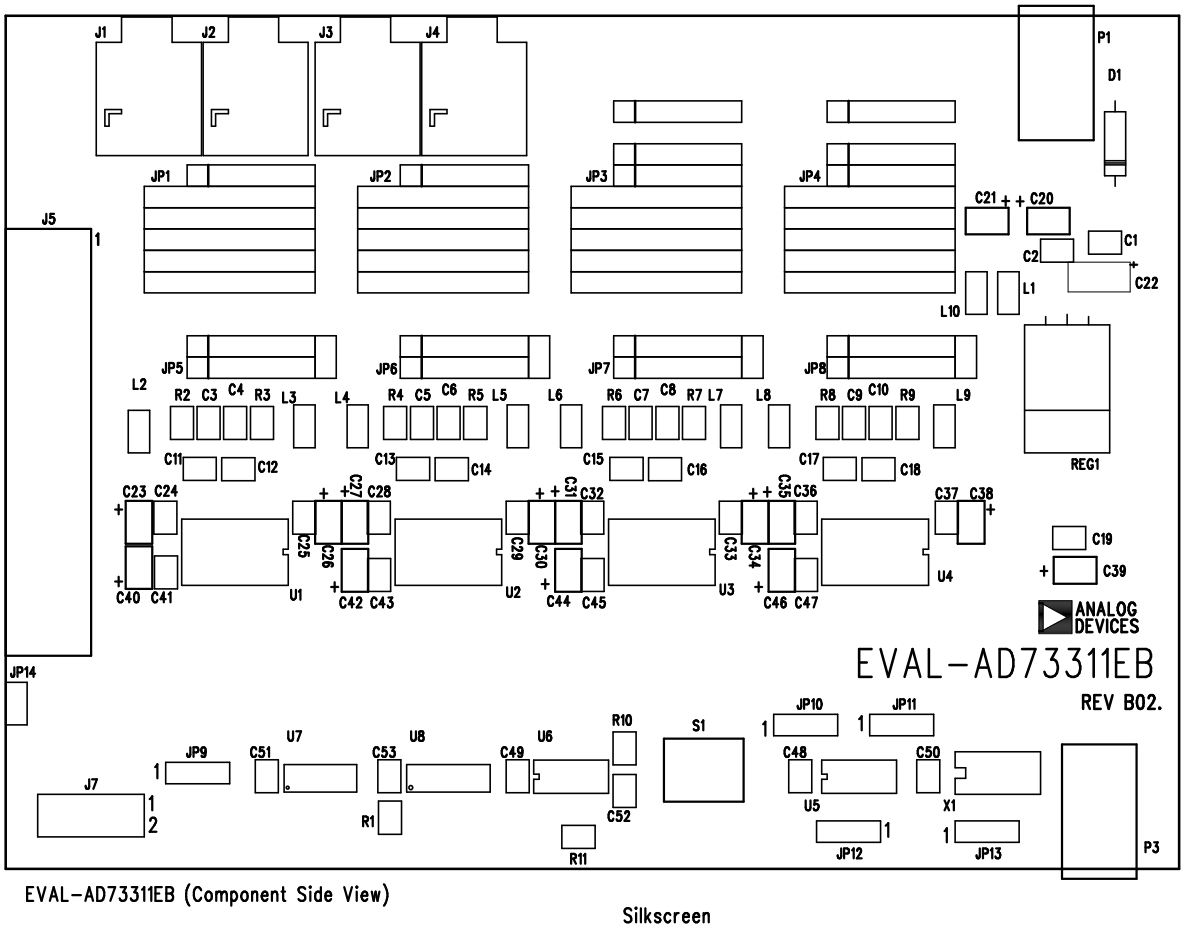
FourChannels (a:\EZ_73311\multi\4in4out.exe)
This program configures a four codec cascade.

NOTE: New demonstration programs and revised versions of existing programs will be available for download at Analog's Website *http://www.analog.com*. Please search for the AD73311 page and choose either the *Evaluation Tools* or *Related Topics* option.

GENERAL NOTES.
The number of devices configured in cascade is programmed using the PF4 and PF5 flag I/O bits from the ADSP-2181. These bits are used to program a 74HC253 dual 4:1 multiplexer which selects the SDO/SDOFS combination from one of the four possible AD73311 codecs on the evaluation board. The settings of PF4 and PF5 for each of the possible cascade configurations is shown in the table below:

PF5	PF4	Cascade Selection
0	0	Single Codec
0	1	Two Codecs
1	0	Three Codecs
1	1	Four Codecs

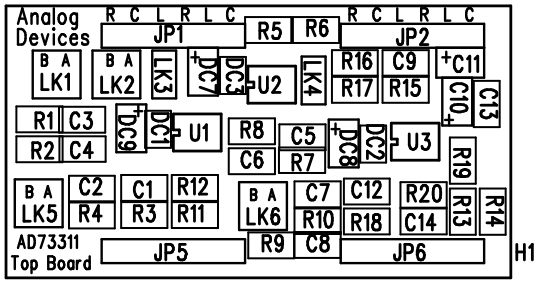
Table I. Program settings for cascade configurations



EVAL-AD73311EB (Component Side View)

Silkscreen

Fig. 3: EVAL-AD73311EB Main Board.



AD73311 Top Board (Component Side View)

Comp Side Silkscreen

Fig. 4: EVAL-AD73311EB Daughter Board.

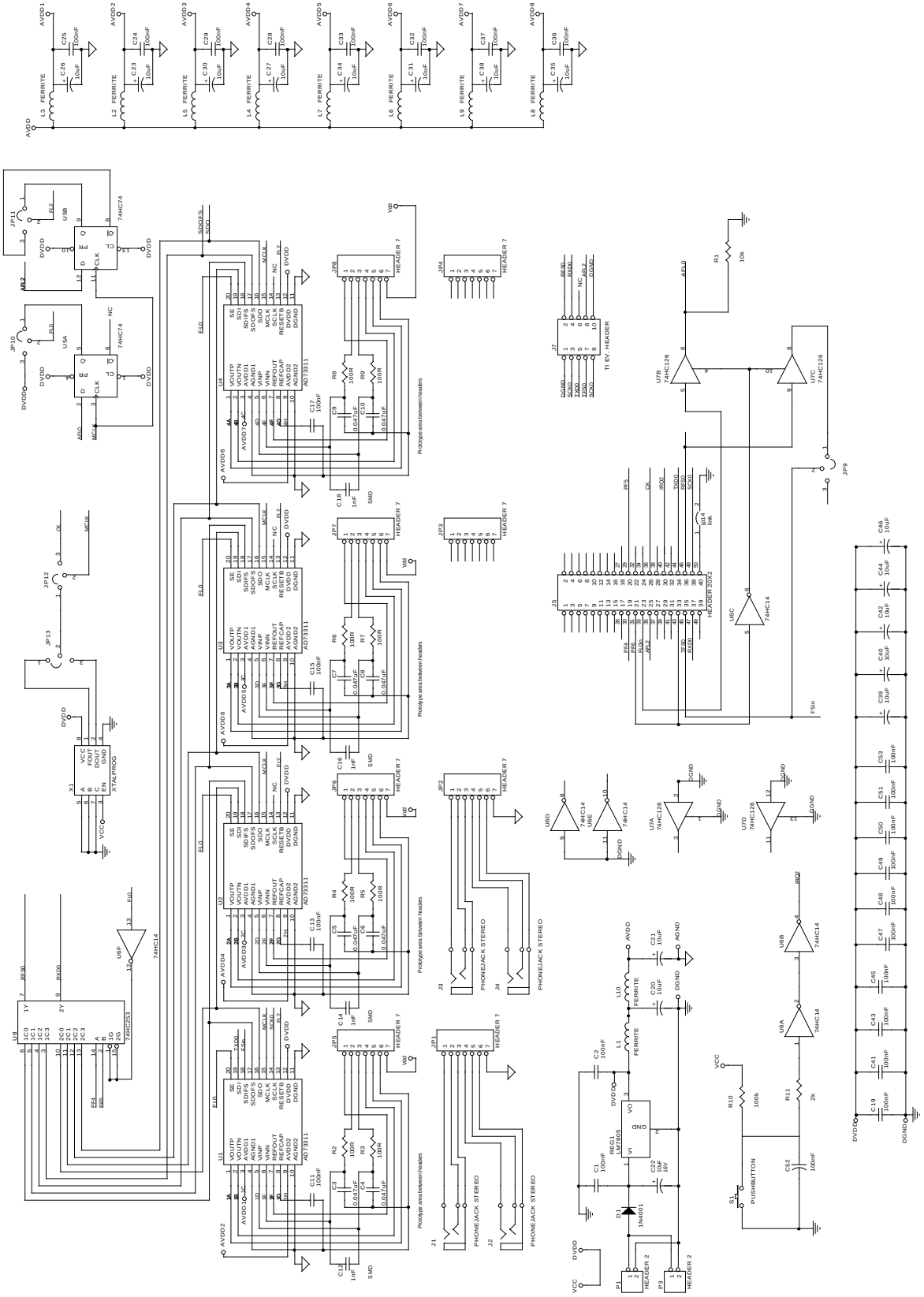


Fig. 5: EVAL-AD73311EB Schematic.

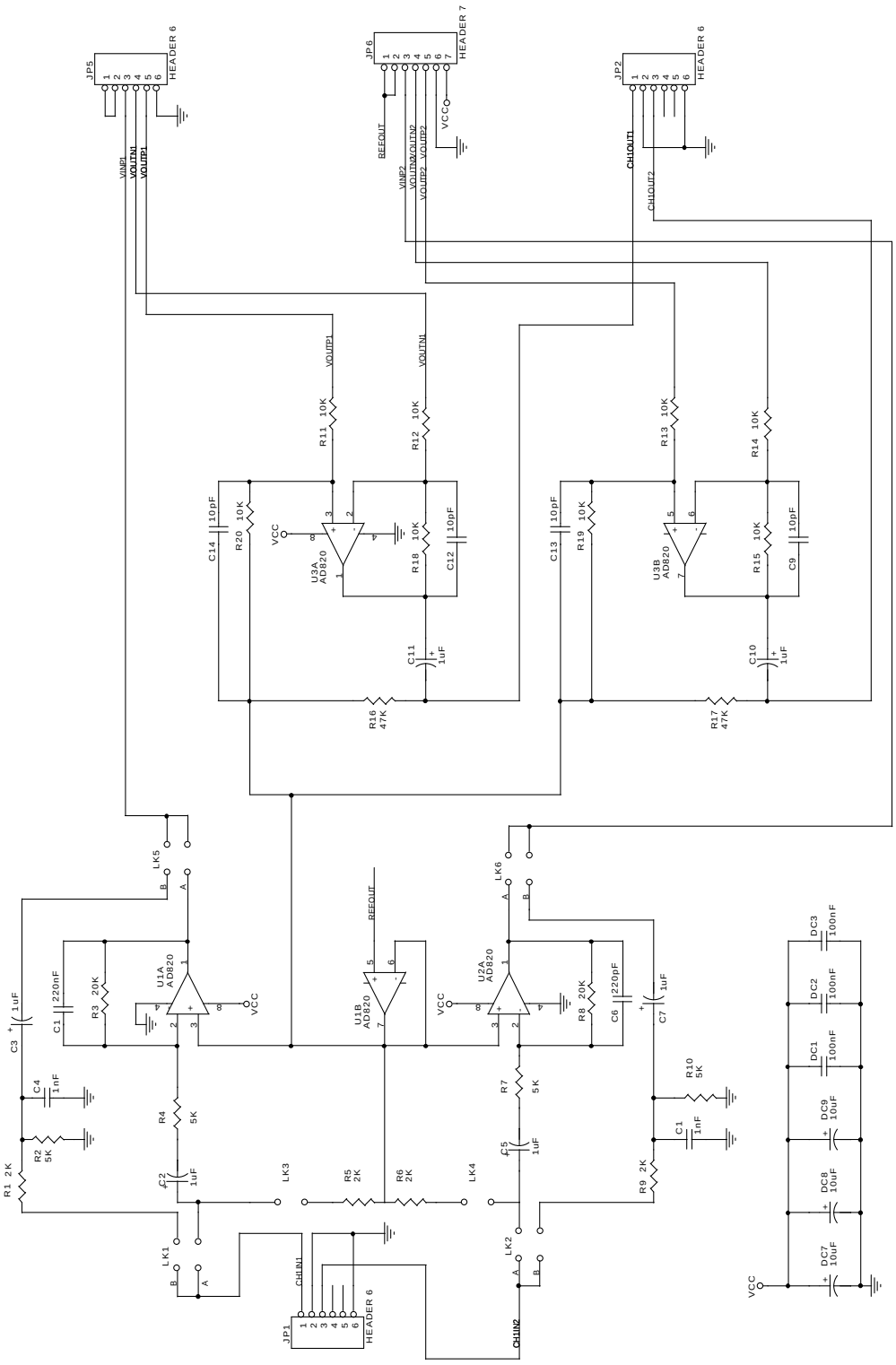


Fig. 6: EVAL-AD73311EB Daughter Board Schematic.

EVAL-AD73311EB (MAIN BOARD) BILL OF MATERIALS.

Intergrated Circuits

Component	Location	Vendor - Part Number
AD73311	U1 U2 U3 U4	Analog Devices -AD73311AR
74HC74D	U5	FEC - 492-358
74HC14D	U6	FEC - 492-310
74HC126D	U7	MOTOROLA - MC74HC126D
74HC253D	U8	MOTOROLA - MC74HC253D
16.384MHz Prog. XTAL	X1	FEC - 221-740
7805CT	REG1	FEC - 701-853
IN4002	D1	FEC - 1N4002

Capacitors

Component	Location	Vendor
100nF 25V X7R (0805)	C1 C2 C11 C13 C15 C17 C19 C24 C25 C28 C29 C32 C33 C36 C37 C41 C43 C45 C47 C48 C49 C50 C51 C52 C53	FEC - 499-687
0.047uF 25V X7R (0805)	C3 C4 C5 C6 C7 C8 C9 C10	FEC - 578-204
Unused Locations	C12 C14 C16 C18	----------
10uF 6.3V TEH-X Tant.	C20 C21 C23 C26 C27 C30 C31 C34 C35 C38 C39 C40 C42 C44 C46	FEC - 286-254
10uF 16V X TEH-C Tant.	C22	FEC - 247-510

Resistors/Inductors

Component	Location	Vendor
10KΩ ±2% 0.1W (0805 Case)	R1	FEC - 109-318
100Ω ±2% 0.1W (0805 Case)	R2 R3 R4 R5 R6 R7 R8 R9	FEC - 109-306
100KΩ ±2% 0.1W (0805 Case)	R10	FEC - 109-324
2.2KΩ ±2% 0.1W (0805 Case)	R11	FEC - 109-314
Ferrite Bead	L1 L2 L3 L4 L5 L6 L7 L8 L9 L10	FEC - 108-267

Connectors / Headers/Links/Switches

Component	Location	Vendor
3 Pole Stereo PCB Socket	J1 J2 J3 J4	FEC - 152-204
Stereo plug	J1 J2 J3 J4	FEC - 152-203 (supply loose with pcb)
Pin Header Socket (Side Entry)	J5	FEC - 148-532
Pin Header (Dual Row) (5+5)	J7	FEC - 511-808
Turned Pin Socket Strip (7way)	JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8	Preci-Dip 801-91-007-10-002
Pin Header (Single Row) (3 way)	JP9 JP10 JP11 JP12 JP13	FEC - 511-717
Pin Header (Single Row) (2 way)	JP14	FEC - 511-705
Shorting Plugs	JP9 JP10 JP11 JP12 JP13 JP14	FEC - 528-456
PCB Mount Power Connector	P1 P3	FEC - 224-959
Power Plug	P1 P3	FEC - 224-923
Push Button Switch	S1	FEC - 176-986

Wire - 30mm strips - Red & Black (attach to power plugs P1 and P3, supply assembled cable with pcb)

EVAL-AD73311EB (DAUGHTER BOARD) BILL OF MATERIALS.

Intergrated Circuits

Component	Location	Vendor - Part Number
AD822AR	U1 U2 U3	Analog Devices -AD822AR

Capacitors

Component	Location	Vendor
220pF (1206 Case)	C1 C6	FEC - 499-286
1uF (1206 Case)	C2 C3 C5 C7	FEC - 499-717
1000pF (1206 Case)	C4 C8	FEC - 499-316
10pF (1206 Case)	C9 C12 C13 C14	FEC - 499-237
1uF (TEH-X Case)	C10 C11	FEC - 247-583
0.1uF (0805 Case)	DC1 DC2 DC3	FEC - 499-687
10uF 6.3V X TEH Tant.	DC7 DC8 DC9	FEC - 286-254

Resistors

Component	Location	Vendor
2KΩ ±2% 0.25W (1206 Case)	R1 R5 R6 R9	FEC - 420-451
5.1KΩ ±2% 0.25W (1206 Case)	R2 R4 R7 R10	FEC - 420-554
20KΩ ±2% 0.25W (1206 Case)	R3 R8	FEC - 420-694
10KΩ ±2% 0.25W (1206 Case)	R11 - R15, R18 - R20	FEC - 420-621
47KΩ ±2% 0.25W (1206 Case)	R16 R17	FEC - 420-785

Connectors / Headers/Links

Component	Location	Vendor
6 Way SIL Header	JP1 JP2 JP5	Preci-Dip 800-10-006-10-002
7 Way SIL Header	JP6	Preci-Dip 800-10-007-10-002
2x2 DIL Pin Header	LK1 LK2 LK5 LK6	FEC - 511-780
1x2 DIL Pin Header	LK3 LK4	FEC - 511-780
Shorting Plugs	LK1 - LK6	FEC - 528-456